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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mn

Office Action Summary	Application No.	Applicant(s)	
	10/518,417	KIKUCHI, SYUICHI	
	Examiner	Art Unit	
	Kalpit Parikh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-26 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-26 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

I. APPLICATION INFORMATION

The instant application having Application No. 10518417 has a total of 25 claims pending in the application; there are 3 independent claims and 22 dependent claims, all of which are ready for examination by the examiner.

Applicants' amendments to the claims have been considered. Applicants have amended claims 1 and 4-25 cancelled claims 2, 3, and 27-31 and added claim 32.

Applicants have amended the each of the independent claims to recite the translation table (support: original claim 17), empty block table (support: PAGE 38 LINES 1-5) and write pointer are stored (support PAGE 17 LINES 13-14) in flash memory. Applicants have further amended the independent claims to recite the limitations of original claims 2 and 3.

II. REJECTIONS NOT BASED ON PRIOR ART

Claim Objections

1. **CLAIM 1** objected to because of the following informalities: Claim 1 recites "constitutesaid" in Claim 1 line 23. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **CLAIMS 8-25** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

CLAIMS 8 recites the limitations "said logical address stored in said page," "a logical address which is associated with the physical address of a page." The claim subsequently recites, "eliminates data stored in a page." It is unclear which page is being referenced by the subsequent limitation.

It is also unclear what elements are being compared (i.e., coincide) as claim 8 has been amended to recite a logical address and a page in an address translation table, a logical address stored in a page and a page whose data is eliminated without reciting a relationship among the elements.

Further claim 8 recites eliminates data when there is no coincidence but does not further disclose what elements are being compared.

Claim 14 recites "said specified value" however no parent claim from which claim 14 depends recites a specified value.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **CLAIMS 1,4-5, 26 AND 32** rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (US Pat No. 6477632, PCT PUB DATE: June 17, 1999) in view of Mason (US Pat No. 5740396) and Sinclair et al. (US Pat No. 6725321).

   As per claims 1, 26, and 32 Kikuchi discloses a memory device comprising:

   - a non-volatile memory (see Kikuchi FIG 3) including a plurality of memory blocks for storing data to which physical addresses are allocated (see Kikuchi FIG 3: 'Blocks'), each of said blocks including physical pages (see Kikuchi FIG 3: 'PAGE'), each of said physical pages including data area and a redundancy portion (see Kikuchi FIG 3: 'REDUNDANT PORTION');
   - a translation table memory which stores an address translation table (BPT) showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages, the translation table memory being comprised of a part of said non-volatile memory (11) (see Kikuchi ABSTRACT);
   - an empty block table memory which stores information (BSI) designating empty blocks which do not store data, said empty block table memory being comprised of a part of said non-volatile memory (11) (see Kikuchi ABSTRACT);

     [Kikuchi discloses the translation table and the empty block table are stored in the flash memory (see ABSTRACT).]

- a controller (12, S311, S314)(see Kikuchi FIG 1: 20) which:
  - o when to-be-written data and a logical address are supplied to said memory device, writes said to-be-written data in the empty page indicated by said write pointer (see Kikuchi COL 3 LINES 13-16), and renews said address translation table in such a way as to show a correlation between the physical address of an empty pare and said logical address (see Kikuchi COL 4 LINES 28-32);
  - o designates memory blocks from which data is to be erased from among memory blocks which have data stored therein (S501) (see Kikuchi FIG 9: S221), and
  - o discriminates whether data stored in said designated memory blocks is valid or not, for each page which constitutes said designated memory blocks, transfers data which has been discriminated as valid to another memory block (S502, S506), and erases data which is stored in said designated memory blocks (S503) (see Kikuchi FIG 9); and

    [Kikuchi discloses identifying a block to be erased, transferring the valid contents of the block to a new location and subsequently erasing the block.]

However Kikuchi do not expressly disclose

- a pointer memory which specifies an empty page in a data storable state from among said pages and stores a write pointer indicating a

physical address of said specified empty page, said pointer memory being comprised of a part of said non-volatile memory (11)

- o discriminates whether or not the number of memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317) using the information stored in said empty block table memory,
- o designates memory blocks from which data is to be erased from among data-storing memory blocks when having discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition (S501).

In the same field of endeavor, Mason discloses a write pointer that is incremented cyclically sector by sector (see Mason COL 6 LINES 62- COL 7 LINES 6). Mason further discloses a step of initiating an erase operation based on an identification that the number of free blocks is below a predetermined threshold (see Mason COL 9 LINES 20-26).

Mason and Kikuchi are analogous art because they are from the same field of endeavor, namely flash memory.

It would have been obvious at the time of invention to implement a flash memory management system as taught by Mason (see Mason FIG 6) into the memory device as taught by Kikuchi (see Kikuchi FIG 1).

The suggestion/motivation for doing so would have been to implement a system that utilized flash memory more efficiently and implemented an address translation table that occupied less space.

Therefore it would have been obvious to a person of ordinary skill in the art to modify Kikuchi to further include an erasure operation as taught by Sinclair for the benefit of guaranteeing a certain amount of free memory blocks to arrive at the invention as specified in the claims.

However, Mason does not expressly disclose the write pointer is stored in the flash memory.

In the same field of endeavor Sinclair et al. disclose storing a sector write pointer in a header of a flash memory block (see COL 13 LINE 29).

It would have been obvious at the time of invention to modify Kikuchi in view of Mason to store the write pointer in the flash memory.

The suggestion/motivation for doing so would have been for the benefit of recovering from an unexpected power loss (see Sinclair et al. COL 28 LINE 67- COL 29 LINE 11)

Therefore it would have been obvious at the time of invention to modify Kikuchi in view of Mason to store the write pointer in flash memory as taught by Sinclair et al. for the benefit of power loss recovery to arrive at the invention as specified in the claims.

As per claim 4, Kikuchi in view of Mason and Sinclair et al. disclose the memory device according to claim 3, wherein said controller (12)

- writes invalid flag indicating that data stored in a page to which a logical address has been allocated at a time-to-be-written data, and said logical address are supplied to said memory device is invalid in the page once (S310) (see Mason COL 9 LINES 28-33), and
- said controller (12) designates an oldest-data storing memory block among data storing blocks which include pages where said invalid flag is written once, as a memory block form which data is to be erased (S501) (see Mason COL 7 LINES 35-49 AND COL 9 LINES 20-27).

  [Mason discloses designating Block 1 as the block to be erased. Block is the oldest storing block that contains invalid data.]

As per claim 5, Kikuchi in view of Mason and Sinclair et al. disclose the memory device according to claim 4, wherein said controller (S502, S506)

- eliminates data stored in a page where said invalid flag is written once from data which are to be transferred to said another memory block (see Mason COL 9 LINES 24-27 AND FIG 13: 37).

  [Invalid data of a block is eliminated because invalid data is not copied to another block before erasing the block.]

6. **CLAIMS 6-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi (US Pat No. 6477632, PCT PUB: 7.17.1999) in view of Mason (US Pat No. 5740396) and Sinclair et al. (US Pat No. 6725321), as applied to claim 1 above, and further in view of Sinclair (US Pat No. 6069827).

   As per claim 6, Kikuchi in view of Mason and Sinclair et al. disclose the memory device according to claim 1,

- wherein a physical address includes a block addresses indicating that a block to which a page indicated by said physical address belongs, and block address are cyclically ordered (see Mason FIG 6: PSA).

  [A physical address of Mason comprises a block address because a block address is required to access the data.]

However neither Kikuchi, nor Mason nor Sinclair et al. disclose

- said controller (S501) designates, as a memory block from which data is to be erased, one of data storing memory block which is or follows a last block where data has been erased and to which a top block address is given.

In the same field of endeavor Sinclair discloses a system where blocks are cyclically ordered and

- a controller designates, as a memory block from which data is to be erased, one of data storing memory block which is or follows a last block where data has been erased and to which a top block address is given (see Sinclair COL 6 LINES 35-36).

  [Sinclair teaches erasing an oldest data storing erase block because Sinclair discloses writing and erasing blocks in a sequential order. Sinclair specifically discloses the next erase block has the next highest block address (i.e., top block address) (see also Kikuchi COL 14 LINES 33-42).]

Sinclair and Kikuchi are analogous art because they are from the same field of endeavor, namely flash memory.

It would have been obvious at the time of invention to modify Kikuchi to implement a garbage collection system as taught by Sinclair (see Sinclair FIG 3).

The suggestion/motivation for doing so would have been for the benefit of a maintaining a threshold amount of available write blocks.

Therefore it would have been obvious at the time of invention to implement an erase pointer that was incremented block by block as taught by Sinclair through a memory address space as taught by Kikuchi and Mason for the benefit of maintaining an amount free memory to arrive at the invention as specified in the claims.

As per claim 7, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 6, wherein said controller (12)

- writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in the page once (S310) (see Mason: COL 9 LINES 28-33), and
- eliminates data stored in the page where said invalid flag is written once from data which are to be transferred to said another memory block (S502, S506) (see Mason: COL 9 LINES 24-27 AND FIG 13: 37).

As per claim 8, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device of claim 6, wherein said controller (12)

- writes a logical address supplied to said memory device in a page where said to-be-written data has been written (S314) (see Mason FIG 4: 12) , and
- discriminates whether or not said logical address stored in said page coincides with a logical address which is associated with the physical address of a page in said address translation table (see Mason FIG 8), and
- eliminates data stored in a page from data which are to be transferred to said another memory block when having discriminated that there is no coincidence (S501, S502, S506) (see Mason FIG 7: 'A').

  [Mason discloses determining if a data is invalid (i.e., discriminating no coincidence between logical address stored and translation table) and if invalid not copying (i.e., eliminating) the data to the new block.]

As per claim 9, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 8,

- wherein physical addresses are cyclically ordered, and said pointer memory (123) specifies a top one of empty pages which are given physical addresses equal to or following the physical address of a page where data is written (see Mason COL 6 LINE 62-COL 7 LINE 6).

  [The physical addresses are cyclically ordered because the physical addresses are represented in a binary numbering scheme, wherein incrementing the highest address outputs the first address because the

number of bits representing the address are fixed (ex/F+1=0) (see Mason COL 6 LINES 30-33.]

As per claim 10, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 9, wherein when

- the logical address of a to-be-read page is supplied to said memory device, a physical address associated with said logical address is specified based on said address translation table and data is read out from a page which is indicated by said specified physical address and is sent outside (S206 to S214) (see Mason FIG 11: 23).

As per claim 11, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 9,

- wherein when the logical address of a to-be-read page is supplied to said memory device, a page which is given said logical address is specified based on said address translation table and data is read out from said specified page and is sent outside (S206 to S214)(see Mason FIG 11: 27).

As per claim 12, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 11, wherein

- said address translation table shows a correlation between predetermined upper digits of the physical address of each page and the logical address of the page,

[Pages addresses are sequentially ordered, so the upper digits of the physical address of each page belonging to the same memory block will have the same upper digits (see Mason FIG 6: 5A 'PBN').]

- said controller (12) writes a logical address supplied to said memory device in a page where said to-be-written data has been written (see Mason FIG 6: Block 3: 7-G-1); and
- when the logical address of a to-be-read page is supplied to said memory device, a value of said predetermined upper digits of the physical address associated with said logical address is specified based on said address translation table (see Mason FIG 6: 5A: Block address is specified) and
- data is read out from that page which is included in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written, and is sent outside (S206 to S214) (see Mason COL 8 LINE 64 - COL 4 LINE 4).

  [Data is read from each page of a block, which contains pages that have a physical address whose upper digits coincide with said specified value.]

As per claim 13, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 12, wherein said controller (12)

- writes an invalid flag indicating that data stored in a page to which a logical address has been allocated at a time to-be-written data and said logical address are supplied to said memory device is invalid in a page once (S310)(see Mason: FIG 6: Block 1-1-A AND Block 1-2-A'), and
- data is read out from a page which is included in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written and said invalid flag is not written, and is sent outside (S206 to S214) (see Mason: COL 7 LINES 55- COL 8 LINE 5 AND COL 6 LINES 48-50).

As per claim 14, , Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 8, wherein

- physical addresses are cyclically ordered, said pointer memory (123) specifies a top one of empty pages which are given physical addresses equal to or following the physical address of a page where data is written (see Mason COL 6 LINE 66-COL 7 LINE 5), and
- said controller (12) reads out data from a lowest-ordered page in individual pages each having a physical address whose upper digits coincide with said specified value and in which said logical address of said to-be-read page is written, and sends said data outside (S206 to S214) (see Mason COL 7 LINE 55- COL 8 LINE 5).

As per claim 15, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 11, wherein

- said address translation table shows a correlation between predetermined lower digits of the physical address of each page and the logical address of the page, and a range over which a value of a physical address can be associated with a logical address is determined for each logical address, (see Mason FIG 5A) and

  [The translation table shows a correlation between the lower digits of the physical address and the logical address because the table shows a correlation between the physical address and the logical address.]
- when the logical address of a to-be-read page is supplied to said memory device, said controller (S206 to S214) specifies a value of said predetermined lower digits of the physical address associated with said logical address is specified based on said address translation table (see Mason FIG 6: 5A LSA->PBN), and
- reads out data from a page which is included in individual pages each having a physical address whose lower digits coincide with said specified value and which is given a physical address lying in said range (see Mason FIG 6: 8A Block 3-Pages 7-9), and sends the data outside (see Mason FIG 6: 8A).

As per claim 16, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 15, wherein

- said translation table memory (123) is constituted by a non-volatile memory which stores said address translation table (see Kikuchi COL 2 LINES 19-21.

As per claim 17, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair the memory device according to claim 15, wherein

- said translation table memory (123) is constituted by the page that stores said address translation table (see Kikuchi COL 2 LINES 19-41), and
- said controller (S310 to S312) reads at least a part of said address translation table from said page (see Kikuchi COL 2 LINES 39-41)
- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address and writes said renewed part in another empty page (S601 to S603)(see Kikuchi FIG 10).

As per claim 18, Kikuchi in view of Mason and Sinclair et al. and further in view of Sinclair disclose the memory device according to claim 17, wherein in that said controller (12)

- stores an address translation table storage location list showing physical addresses of pages which store data constituting said address translation table (S105B) (see Kikuchi COL 8 LINES 53-64),

- reads at least a part of said address translation table from a page which is given a physical address indicated by said address translation table storage location list (see Kikuchi FIG 6:103),
- renews said read part in such a way as to show a correlation between the physical address of said empty page indicated by said write pointer and said logical address (see Kikuchi FIG 12) and
- writes said renewed part in another empty page (see Mason FIG 10), and
- renews said address translation table storage location list in such a way as to show the physical address of said another empty page (S602, S603) (see Kikuchi FIG 10 S316).

IV. **ALLOWABLE SUBJECT MATTER**

7. **CLAIMS 19-25** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The primary reasons for allowance of claims 19-25 in the instant application is the combination with the inclusion in these claims that

> "said controller (12) stores an address translation table storage location list showing predetermined lower digits of the physical address of each of pages which store data constituting said address translation table (S 105B), reads at least a part of said address translation table from ~ a page which is included in pages each having a physical address whose predetermined lower digits are specified by said address translation table storage location list and the predetermined upper digits of the physical address of which lies in said range, renews said read part in such a way as to show a correlation."

The prior art of record neither anticipates nor renders obvious the above recited combination. Rather Kikuchi (primary reference) discloses storing the address translation table at arbitrary locations.

If the applicant should choose to rewrite the independent claims to include the limitations recited in either one of claims 19-25, the applicant is encouraged to amend the title of the invention such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the Summary of the Invention and the Abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the M.P.E.P

V. **ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT**

Applicants' arguments filed May 21, 2007 have been fully considered but they are not deemed persuasive. A response to Applicants' argument appears below.

WITHDRAWN IN VIEW OF APPLICANTS AMENDMENTS:

Double Patenting Rejection of CLAIMS 1-31 over copending Application No. 11/547181.

RESPONSE TO AMENDMENTS/ARGUMENTS

1st POINT OF ARGUMENT:

Applicants have argued no combination of the references (i.e., Kikuchi, Sinclair, Mason, Sinclair et al.) teaches storing a translation table, empty block table, and write pointer in the nonvolatile memory.

Applicants are respectfully pointed to Sinclair et al., which teaches a translation table (i.e., SAT) (see COL 2 LINES 7-22), write pointer (COL 13 LINE 29) and a map of the empty blocks (see COL 11 LINES 46-49) in the non-volatile memory.

Further Kikuchi discloses storing an empty block table that points to a next write block address, and a translation table in flash memory (see ABSTRACT AND Kikuchi COL 14 LINES 33-42). While the write pointer of Kikuchi may be construed as pointing in units of blocks rather than sectors, implementing a write pointer that points to a sector would have been obvious (see e.g., Motivation: Mason COL 6 LINES 62-COL 7 LINES 6).

2nd POINT OF ARGUMENT:

Applicants have argued that the method by which Sinclair designates blocks is different from the designation method as claimed.

It is unclear on what grounds Applicants regard the claimed designation method different from the method disclosed by Sinclair, because Applicants do not further elaborate on the matter.

The claim as recited appears to state the controller designates, as the next eligible block that may be erased, a block with the next highest address (i.e., top block address).

Sinclair discloses an erase pointer that is sequentially incremented to point to a block that may be erased.

Sinclair is understood to teach the limitation because Sinclair discloses an erase pointer that is incremented sequentially to point to the next eligible erase block. A sequential address is understood to be the next highest address (see also Sinclair COL 6 LINES 24-29).

3rd POINT OF ARGUMENT:

Applicants have argued the combination of Mason and Sinclair cannot be enabled.

Applicants have argued the manner for designating an erase block in Mason and Sinclair is different.

Sinclair is relied upon to teach an erase pointer that may be incremented sequentially through an address space.

Sinclair discloses an erase pointer that may be incremented to point to a block and a write pointer that may be incremented to point to a sector. Mason discloses flash memory that is block addressable and further includes a write pointer that may be incremented sector by sector. Mason discloses the memory is flash memory.

An erase pointer implemented in Mason is understood to point to block addresses, such as those stored in the translation table. It is unclear why implementing an erase pointer into a system as disclosed by Mason cannot be enabled.

VI. **CLOSING COMMENTS**

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

Per the instant office action, claims 1,4-25,26, and 32 have received a second action on the merits and are subject of a final action.

VIa. **CLAIMS REJECTED IN THE APPLICATION**

For at least the above reasons it is the examiner's position that the applicant's claims 1,4-25,26, and 32 are not in condition for allowance.

VII. **DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kalpit Parikh/

Kalpit Parikh
Examiner
Art Unit 2187

July 30, 2007

DONALD SPARKS
SUPERVISORY PATENT EXAMINER